REMARKS

This Amendment responds to the Office Action dated May 5, 2004 in which the Examiner objected to the abstract, rejected claims 1 and 4-5 under 35 U.S.C. §102(e) and rejected claims 2-3 under 35 U.S.C. §103.

As indicated above, the abstract has been amended to a single paragraph. Applicant respectfully requests the Examiner approves the correction and withdraws the objection to the abstract.

As indicated above, claim 1 has been amended to make explicit what is implicit in the claims. Applicant respectfully submits that the amendment is unrelated to a statutory requirement for patentability and does not narrow the literal scope of the claim.

Claim 1 claims an integrated circuit device comprising an integrated circuit, an insulator and at least one connection pile. The integrated circuit is formed on a first surface of a substrate. The insulator is formed on a second surface opposed to the first surface of the substrate. The at least one connection pile is made of a conductive material filled up in a corresponding unlined hole which is so formed that the hole penetrates the substrate, the integrated circuit, and the insulator.

Through the structure of the claimed invention having at least one connection pile made of a conductive material filled up in a corresponding unlined hole which is so formed that it penetrates the substrate, the integrated circuit and the insulator, as claimed in claim 1, the claimed invention provides an integrated circuit device capable of preventing any occurrence of an electrical connection between circuits formed in integrated circuit of upper and lower layers in a multilayer structure. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claims 1 and 4-5 were rejected under 35 U.S.C. §102(e) as being anticipated by *Cote et al* (U.S. Patent No. 6,548,901). In addition, claims 2-3 were rejected under 35 U.S.C. §103 as being unpatentable over *Cote et al.*

Cote et al appears to disclose an interconnect structure, including multilevel interconnect structures, in which dense fringing fields typically present at the bottom corners of the interconnect regions are significantly reduced. (col. 1, lines 7-10) Reference is first made to FIG. 2 which illustrates a basic interconnect structure which includes substrate 50 and first interconnect level 52. In the embodiments shown in FIGS. 2-3a-b, substrate 50 is a Si-containing material, while in FIGS. 4a-f, 50 is an underlying interconnect level. First interconnect level 52 is comprised of hybrid dielectric 54 and low-k interlayer dielectric layer 56. In accordance with the embodiment shown in FIG. 2, which represents a preferred embodiment of the present invention, metallic lines 60 containing a liner material 70 are present in low-k interlayer dielectric layer 56 so that top horizontal portions 61 of the metallic lines are coplanar with the top surface of low-k interlayer dielectric 56 and that bottom horizontal portions 62 of the metallic lines are not coincident, i.e., non-coplanar, with interface 55 that exists between the two different dielectric layers of the dielectric stack. (col. 4, lines 22-40) Interface 55 which exists between the two dielectric layers is a flat, planar interface in which no notches are present therein. A diffusion barrier layer 64 is shown on first interconnect level 52. (col. 4, lines 50-54) For clarity, region 64 is used herein to include a diffusion barrier and a metallic barrier cap layer as well as combinations thereof. (col. 4, lines 58-60) FIG. 3a shows a multilevel interconnect structure including interconnect levels 52a, 52b and 52c, respectively. Each interconnect level of the illustrated structure is separated by a

barrier layer 64 and is comprised of the same elements as shown in FIG. 2. In addition to those elements, the structure shown in FIG. 3a includes metallic filled vias 66 formed in interconnect levels 52b and 52c which are in electrical contact with the metallic lines 60 of interconnect levels 52a and 52b, respectively. Common to the inventive structures shown in FIGS. 2 and 3a is that top horizontal portions of the metallic lines are coplanar with the top surface of the low-k interlayer dielectric; that the metallic lines are contained within said low-k interlayer dielectric; and that the bottom horizontal portions of the metallic lines are not coincident with the planar interface that exists between the different dielectrics of the dielectric stack. (col. 4, lines 66 through col. 5, line 14)

Thus, *Cote et al* merely discloses metallic lines 60 containing a liner material 70. Nothing in *Cote et al* shows, teaches or suggests at least one conductive pile made of a conductive material filled up in a corresponding unlined hole as claimed in claim 1. Rather, *Cote et al* teaches away from the claimed invention since the metallic lines 60 contain a liner material 70.

Since nothing in *Cote et al* shows, teaches or suggests at least one connection pile made of a conductive material filled up in a corresponding unlined hole as claimed in claim 1, applicant respectfully requests the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(e).

Claims 2-5 depend from claim 1 and recite additional features. Applicant respectfully submits that claims 4-5 would not have been anticipated by *Cote et al* within the meaning of 35 U.S.C. §102(e) and that claims 2-3 would not have been obvious over *Cote et al* under 35 U.S.C. §103 at least for the reasons as set forth above. Therefore, applicant respectfully requests the Examiner withdraws the

rejection to claims 4-5 under 35 U.S.C. §102(e) and withdraws the rejection to claims 2-3 under 35 U.S.C. §103.

New claims 6-9 have been added and recite additional features. Applicant respectfully submits that these claims are also in condition for allowance.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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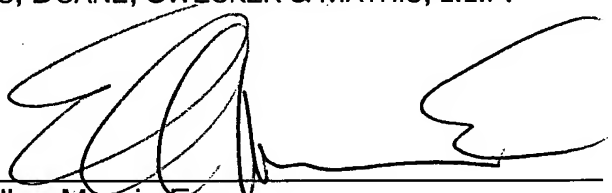

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